(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 May 2006 (18.05.2006)

PCT

(10) International Publication Number
WO 2006/053036 A2

(51) International Patent Classification:
H01L 23/31 (2006.01) *H01L 23/485* (2006.01)

(21) International Application Number:
PCT/US2005/040584

(22) International Filing Date:
8 November 2005 (08.11.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/626,802 10 November 2004 (10.11.2004) US

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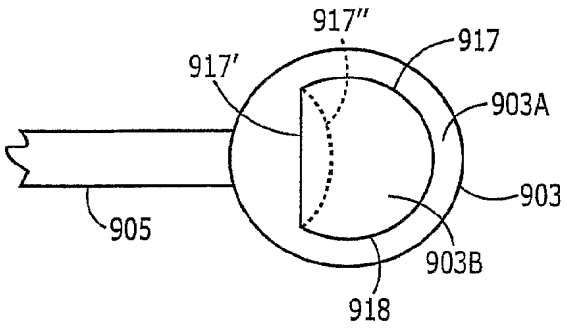
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: NON-CIRCULAR VIA HOLES FOR BUMPING PADS AND RELATED STRUCTURES



(57) Abstract: An integrated circuit device may include a substrate, a conductive pad on a surface of the substrate, and a conductive line on the surface of the substrate. Moreover, the conductive line may be connected to the conductive pad, and the conductive line may be narrow relative to the conductive pad. In addition, an insulating layer may be provided on the substrate, on the conductive line, and on edge portions of the conductive pad. The insulating layer may have a hole therein exposing a central portion of the conductive pad, and a first segment of a perimeter of the hole may substantially define an arc of a circle around the central portion of the conductive pad. A second segment of the perimeter of the hole may substantially deviate from the circle around the central portion of the conductive pad, and the second segment of the perimeter of the hole may be adjacent a connection between the conductive line and the conductive pad.

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NON-CIRCULAR VIA HOLES FOR BUMPING PADS AND RELATED STRUCTURES

Related Applications

[0001] The present application claims the benefit of priority as a Continuation-In-Part (CIP) application from U.S. Utility Application No. 11/226,569 filed September 14, 2005, which claims the benefit of priority as a Divisional application from U.S. Utility Patent Application No. 10/601,938 filed June 23, 2003, which claims the benefit of priority from U.S. Provisional Application No. 60/391,511 filed June 25, 2002. The present application also claims the benefit of priority from U.S. Provisional Application No. 60/626,802 filed November 10, 2004. The disclosures of each of the above referenced utility and provisional applications are hereby incorporated herein in their entirety by reference.

Field of the Invention

[0002] The present invention relates to the field of electronics, and more particularly to electronic structures including solder layers and related methods.

Background

[0003] Solder layers may be used to provide electrical and mechanical coupling between two electronic substrates, such as in flip-chip bonding. In particular, a solder layer may be provided on a conductive pad of an electronic substrate (such as an input/output pad of an integrated circuit substrate), and the solder layer can be used to bond the electronic substrate to a next level of packaging such as a printed circuit board, a ceramic substrate, and/or another integrated circuit device. Accordingly, the solder layer may provide an electrical interconnection between the electronic substrate and the next level of packaging.

[0004] More particularly, a solder bump may be provided on a portion of a conductive pad exposed through a via in an insulating layer. In addition, a relatively thin underbump metallurgy (UBM) layer may promote adhesion, provide a plating electrode,

and/or provide a routing conductor. An insulating layer on the electronic structure may include a via therein exposing a portion of the conductive pad on which the solder layer is provided. As current flowing in a conventional structure reaches an edge of a solder bump via, a lower resistance of the bump may cause most of the current to turn the corner at the via edge. A non-uniform current density may result, and a non-uniform current density may reduce reliability.

[0005] More particularly, a relatively high current density at the via edge may accelerate local electromigration of the solder layer at the via edge. Solder, for example, may be particularly susceptible to electromigration because of its relatively low melting temperature. Diffusion of metal in the solder layer away from the via edge may result in formation of a void in the solder layer adjacent the via edge. The void may block current flow thus forcing the current to travel farther past the via edge before turning toward the solder. Accordingly, a void may grow laterally along an interface between the solder and the conductive pad.

[0006] Solder layers may be relatively sensitive to electromigration as discussed, for example, by W. J. Choi et al. in "Electromigration Of Flip Chip Solder Bump On Cu/Ni(V)/Al Thin Film Under Bump Metallization" (Proceedings of the IEEE Electronic Components Technology Conference, 2002). The disclosure of the Choi et al. reference is hereby incorporated herein in its entirety by reference.

Summary

[0007] According to some embodiments of the present invention, an integrated circuit device may include a substrate, a conductive pad on a surface of the substrate, and a conductive line on the surface of the substrate. The conductive line may be connected to the conductive pad, and the conductive line may be narrow relative to the conductive pad. An insulating layer may be provided on the substrate, on the conductive line, and on edge portions of the conductive pad, and the insulating layer may have a hole therein exposing a central portion of the conductive pad. In addition, a first segment of a perimeter of the hole may substantially define an arc of a circle around the central portion of the conductive pad, and a second segment of the perimeter of the hole may substantially deviate from the circle around the central portion of the conductive pad.

Moreover, the second segment of the perimeter of the hole may be adjacent a connection between the conductive line and the conductive pad.

[0008] A conductive bump may be provided on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the insulating layer is between the conductive bump and edge portions of the conductive pad. Moreover, the conductive bump may include a solder bump, and/or the conductive bump may have a substantially circular footprint on the insulating layer. In addition, an underbump metallurgy layer may be provided on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the under bump metallurgy layer is between the conductive bump and portions of the insulating layer surrounding the hole, and the underbump metallurgy layer and the conductive bump may comprise different materials.

[0009] An input/output pad may be provided on the substrate, and the conductive line may provide electrical connection between the conductive pad and the input/output pad. In addition, a second conductive line may be connected to the input/output pad, and a second conductive pad may be connected to the second conductive line wherein the insulating layer has a second hole therein exposing a central portion of the second conductive pad. In addition, a first conductive bump may be provided on the central portion of the first conductive pad and on portions of the insulating layer surrounding the first hole, and a second conductive bump may be provided on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole.

[0010] According to some embodiments of the present invention, the second segment of the perimeter of the hole may substantially define a line, and a length of the second segment may be at least as great as a width of the conductive line. According to other embodiments of the present invention, the second segment of the perimeter of the hole may curve toward the center of the conductive pad.

[0011] According to additional embodiments of the present invention, an integrated circuit device may include a substrate, a conductive pad on a surface of the substrate, and a conductive line on the surface of the substrate. The conductive line may be connected to the conductive pad, and the conductive line may be narrow relative to the

conductive pad. An insulating layer may be provided on the substrate, on the conductive line, and on edge portions of the conductive pad, the insulating layer may have a hole therein exposing a central portion of the conductive pad, and at least a segment of a perimeter of the hole may be non-circular. In addition, a conductive bump may be provided on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the insulating layer is between the conductive bump and edge portions of the conductive pad and so that the conductive bump has a substantially circular footprint on the insulating layer.

[0012] More particularly, the conductive bump may include a solder bump. In addition, an underbump metallurgy layer may be provided on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the under bump metallurgy layer is between the conductive bump and portions of the insulating layer surrounding the hole. Moreover, the underbump metallurgy layer and the conductive bump may include different materials.

[0013] A first segment of a perimeter of the hole may substantially define an arc of a circle around the central portion of the conductive pad, and a second segment of the perimeter of the hole may substantially deviate from the circle around the central portion of the conductive pad. The second segment of the perimeter of the hole may be adjacent a connection between the conductive line and the conductive pad. According to some embodiments of the present invention, the second segment of the perimeter of the hole may substantially define a line, and a length of the second segment may be at least as great as a width of the conductive line. In other embodiments of the present invention, the second segment of the perimeter of the hole may curve toward the center of the conductive pad. Moreover, an input/output pad may be provided on the substrate wherein the conductive line provides electrical connection between the conductive pad and the input/output pad.

[0014] In addition, the integrated circuit device may include a second conductive line connected to the input/output pad, and a second conductive pad connected to the second conductive line wherein the insulating layer has a second hole therein exposing a central portion of the second conductive pad. A first conductive bump may be provided on the central portion of the first conductive pad and on portions of the

insulating layer surrounding the first hole, and a second conductive bump may be provided on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole.

[0015] According to additional embodiments of the present invention, an integrated circuit device may include a substrate, an input/output pad on the substrate, and first and second conductive lines on the substrate with both of the first and second lines being connected to the input/output pad. First and second conductive pads may be provided on the substrate with the first conductive pad being connected to the first conductive line and with the second conductive pad being connected to the second conductive line. An insulating layer may be provided on the first and second conductive lines and on edge portions of the first and second conductive pads, and the insulating layer may have first and second holes therein exposing central portions of the respective first and second conductive pads. In addition, a first conductive bump may be provided on the central portion of the first conductive bump and on portions of the insulating layer surrounding the first hole, and a second conductive bump may be provided on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole.

[0016] The first and second conductive bumps may include respective first and second solder bumps, and each of the first and second conductive bumps may have a substantially circular footprint on the insulating layer. In addition, a first underbump metallurgy layer may be provided on the central portion of the first conductive pad and on portions of the insulating layer surrounding the first hole so that the first under bump metallurgy layer is between the first conductive bump and portions of the insulating layer surrounding the first hole, and the first underbump metallurgy layer and the first conductive bump may include different materials. A second underbump metallurgy layer may be provided on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole so that the second under bump metallurgy layer is between the second conductive bump and portions of the insulating layer surrounding the second hole, and the second underbump metallurgy layer and the second conductive bump may include different materials.

[0017] The first conductive line may provide a first electrical resistance between the input/output pad and the first conductive pad, the second conductive line may provide a second electrical resistance between the input/output pad and the second conductive pad, and the first and second electrical resistances may be different. According to some embodiments of the present invention, the first conductive line may have a first length between the input/output pad and the first conductive pad, the second conductive line may have a second length between the input/output pad and the second conductive pad, and the first and second lengths may be different. According to some other embodiments of the present invention, the first conductive line may have a first width, the second conductive line may have a second width, and the first and second widths may be different. According to still other embodiments of the present invention, the first conductive line may have a first thickness, the second conductive line may have a second thickness, and the first and second thicknesses may be different. According to yet other embodiments of the present invention, the first conductive line may include a first material, the second conductive line may include a second material, and the first and second materials may be different.

[0018] The input/output pad may be a ground pad providing a ground connection for the integrated circuit device, or the input/output pad may be a power pad providing a power connection for the integrated circuit device. The first conductive line may be narrow relative to the first conductive pad, a first segment of a perimeter of the first hole may substantially define an arc of a circle around the central portion of the first conductive pad, and a second segment of the perimeter of the first hole may substantially deviate from the circle around the central portion of the conductive pad. Moreover, the second segment of the perimeter of the first hole may be adjacent a connection between the conductive line and the conductive pad. Moreover, at least a segment of a perimeter of the first hole may be non-circular.

Brief Description Of The Drawings

[0019] Figure 1A is a top view illustrating a conductive line and pad according to embodiments of the present invention.

[0020] Figures 1B-C are cross sectional views illustrating conductive lines and pads according to embodiments of the present invention.

[0021] Figure 2A is a top view illustrating current concentrations on a conductive line and pad according to embodiments of the present invention.

[0022] Figure 2B is a mapping of greyscale shades from Figure 2A with respect to current densities.

[0023] Figures 3A-B are cross sectional views illustrating power bumps according to embodiments of the present invention.

[0024] Figures 4A-B are cross sectional views illustrating ground bumps according to embodiments of the present invention.

[0025] Figures 5A-B are respective top and cross sectional views illustrating multiple bumps connected to an input/output pad according to some embodiments of the present invention.

[0026] Figures 6A-B are respective top and cross sectional views illustrating multiple bumps connected to an input/output pad according to some other embodiments of the present invention.

[0027] Figures 7A-B are respective top and cross sectional views illustrating multiple bumps connected to an input/output pad according to some additional embodiments of the present invention.

[0028] Figures 8A-B are respective top and cross sectional views illustrating multiple bumps connected to an input/output pad according to some more embodiments of the present invention.

[0029] Figures 9A-B are respective top and cross sectional views illustrating multiple bumps connected to an input/output pad according to still more embodiments of the present invention.

[0030] Figures 10A-B are respective top and cross sectional views illustrating multiple bumps connected to an input/output pad according to yet more embodiments of the present invention.

Detailed Description

[0031] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0032] In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when an element such as a layer, region or substrate is referred to as being on another element, it can be directly on the other element or intervening elements may also be present. In contrast, if an element such as a layer, region or substrate is referred to as being directly on another element, then no other intervening elements are present. Similarly, when an element such as a layer, region or substrate is referred to as being coupled or connected to/with another element, it can be directly coupled or connected to/with the other element or intervening elements may also be present. In contrast, if an element such as a layer, region or substrate is referred to as being directly coupled or connected to/with another element, then no other intervening elements are present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. The symbol "/" is also used as a shorthand notation for "and/or".

[0033] Embodiments of the invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments (and intermediate structures) of the invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes

place. Moreover, a patterned feature (such as a perimeter of a hole) illustrated having sharp transitions may typically have a rounded or curved transition. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of the invention.

[0034] Furthermore, relative terms, such as beneath, upper, lower, top, and/or bottom may be used herein to describe one element's relationship to another element as illustrated in the figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures. For example, if the device in one of the figures is turned over, elements described as below other elements would then be oriented above the other elements. The exemplary term below, can therefore, encompasses both an orientation of above and below.

[0035] It will be understood that although the terms first and second are used herein to describe various regions, layers and/or sections, these regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second region, layer or section could be termed a first region, layer or section without departing from the teachings of the present invention. Like numbers refer to like elements throughout.

[0036] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes", and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0037] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms,

such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0038] Several approaches are discussed to reduce electromigration. According to embodiments of the present invention, effects of electromigration can be reduced by using more power or ground bumps depending on an expected operating temperature of a solder bump interconnection (such as a SnPb solder bump interconnection) because segregation of lead and tin may be a risk at the cathode below 100 degrees C and at the anode above 100 degrees C due to the relative diffusivities of the two components.

[0039] More particularly, diffusivities of lead and tin in a lead-tin solder may vary over temperature, with lead diffusing faster than tin at temperatures greater than approximately 100 degrees C and with tin diffusing faster than lead at temperatures less than approximately 100 degrees C. Moreover, a faster diffusing component of the solder metallurgy may tend to segregate toward a positive terminal (i.e., an anode) of the solder bump, and/or a slower diffusing component of the solder metallurgy may tend to segregate toward a negative terminal (i.e., a cathode) of the solder bump. An increased tin concentration may damage an under bump metallurgy layer between a lead-tin solder bump and a contact pad of an integrated circuit device.

[0040] As shown in Figures 3A-B, a power bump may be connected between a power supply conductor (anode) of a printed circuit board and a Vcc pad (cathode) of an integrated circuit device. As shown in Figure 3A, above approximately 100 degrees C, tin may segregate toward the Vcc pad of the integrated circuit device, and lead may segregate toward the power supply conductor of the printed circuit board. As shown in Figure 3B, below approximately 100 degrees C, lead may segregate toward the Vcc pad of the integrated circuit device, and tin may segregate toward the power supply conductor of the printed circuit board. According to embodiments of the present invention, a plurality of power bumps may be provided for an integrated circuit device when operating conditions for the integrated circuit device are generally expected to exceed approximately 100 degrees C. For example, a plurality of redistribution lines may

connect a respective plurality of solder bumps to a single power pad of the integrated circuit device.

[0041] If operating conditions for an integrated circuit device are generally expected to exceed approximately 100 degrees C, a number of power bumps provided for the integrated circuit device may exceed a number of ground bumps provided for the integrated circuit device. While particular embodiments of the present invention have been discussed with respect to binary solid solution solders such as lead-tin solders, other solid solution solders (including higher order solid solution solders) may be used. Moreover, binary and higher order intermetallic compound solders such as tin-silver and tin-silver-copper solders may also be used according to embodiments of the present invention.

[0042] As shown in the top view of Figure 5A and in the corresponding cross sectional view of Figure 5B, for example, a plurality of redistribution lines **1111A-C** may connect a respective plurality of solder bumps **1115A-C** to a single Vcc pad **1117** of the integrated circuit device, and each redistribution line **1111A-C** may include a respective pad portion **1111A'**, **1111B'**, and **1111C'**. More particularly, the integrated circuit device may include a semiconductor substrate **1119**, a first insulating layer **1121**, and a second insulating layer **1123**. The redistribution lines **1111A-C** may be provided between the first and second insulating layers **1121** and **1123**, and via holes in the second insulating layer **1123** may expose pad portions **1111A'**, **1111B'**, and **1111C'** of the redistribution lines **1111A**, **1111B**, and **1111C**. In addition, a respective under bump metallurgy layer **1125** may be provided between each of the solder bumps **1115A-C** and the pad portions **1111A'**, **1111B'**, and **1111C'** of the redistribution lines. The under bump metallurgy layer **1125B** is shown in the cross sectional view of Figure 5B.

[0043] In addition or in an alternative, a plurality of solder bumps may be connected to a respective plurality of Vcc pads. By providing a plurality of power bumps, current can be distributed, and segregation can be reduced. Moreover, failure of a single power bump may not be catastrophic.

[0044] While not shown in Figures 5A-B, one or more of the via holes through the insulating layer **1123** exposing conductive pads **1111A'**, **1111B'**, and/or **1111C'** may have a non-circular perimeter as discussed below with respect to Figures

1A-C. More particularly, one or more of the via holes through the insulating layer **1123** exposing one or more of conductive pads **1111A'**, **1111B'**, and/or **1111C'** may have a "D" shaped and/or a crescent shaped perimeter as discussed below with respect to Figures 1A-C.

[0045] As shown in Figures 4A-B, a ground bump may be connected between a ground conductor (cathode) of a printed circuit board and a ground pad (anode) of an integrated circuit device. As shown in Figure 4A, above approximately 100 degrees C, lead may segregate toward the ground pad of the integrated circuit device, and tin may segregate toward the ground conductor of the printed circuit board. As shown in Figure 4B, below approximately 100 degrees C, tin may segregate toward the ground pad of the integrated circuit device, and lead may segregate toward the ground conductor of the printed circuit board. According to embodiments of the present invention, a plurality of ground bumps may be provided for an integrated circuit device when operating conditions for the integrated circuit device are generally expected not to exceed approximately 100 degrees C. For example, a plurality of redistribution lines may connect a respective plurality of solder bumps to a single ground pad of the integrated circuit device.

[0046] If operating conditions for an integrated circuit device are generally expected not to exceed approximately 100 degrees C, a number of ground bumps provided for the integrated circuit device may exceed a number of power bumps provided for the integrated circuit device. While particular embodiments of the present invention have been discussed with respect to binary solid solution solders such as lead-tin solders, other solid solution solders (including higher order solid solution solders) may be used. Moreover, binary and higher order intermetallic compound solders such as tin-silver and tin-silver-copper solders may also be used according to embodiments of the present invention.

[0047] As shown in the top view of Figure 6A and in the corresponding cross sectional view of Figure 6B, for example, a plurality of redistribution lines **2111A-C** may connect a respective plurality of solder bumps **2115A-C** to a single ground pad **2117** of the integrated circuit device, and each redistribution line **2111A-C** may include a respective pad portion **2111A'**, **2111B'**, and **2111C'**. More particularly, the integrated

circuit device may include a semiconductor substrate **2119**, a first insulating layer **2121**, and a second insulating layer **2123**. The redistribution lines **2111A-C** may be provided between the first and second insulating layers **2121** and **2123**, and via holes in the second insulating layer **2123** may expose pad portions **2111A'**, **2111B'**, and **2111C'** of the redistribution lines **2111A**, **2111B**, and **2111C**. In addition, a respective under bump metallurgy layer **2125** may be provided between each of the solder bumps **2115A-C** and the pad portions **2111A'**, **2111B'**, and **2111C'** of the redistribution lines. The under bump metallurgy layer **2125B** is shown in the cross sectional view of Figure 6B.

[0048] While not shown in Figures 6A-B, one or more of the via holes through the insulating layer **2123** exposing conductive pads **2111A'**, **2111B'**, and/or **2111C'** may have a non-circular perimeter as discussed below with respect to Figures 1A-C. More particularly, one or more of the via holes through the insulating layer **2123** exposing one or more of conductive pads **2111A'**, **2111B'**, and/or **2111C'** may have a "D" shaped and/or a crescent shaped perimeter as discussed below with respect to Figures 1A-C.

[0049] In addition or in an alternative, a plurality of solder bumps may be connected to a respective plurality of ground pads. By providing a plurality of ground bumps, current can be distributed, and segregation can be reduced. Moreover, failure of a single ground bump may not be catastrophic.

[0050] Benefits may also be provided according to embodiments of the present invention by connecting a plurality of solder bumps to input/output pads other than ground and/or Vcc pads. As discussed above with respect to ground and Vcc pads, current can be distributed and segregation can be reduced, and failure of a single bump may not be catastrophic. Provision of multiple bumps may be particularly, beneficial with input/output pads carrying currents sufficient to result in accumulation of vacancies at interfaces between a solder bump and its under bump metallurgy. For example, provision of multiple bumps may be beneficial where relatively large DC currents are provided through a pad (such as a ground and/or Vcc pad). Provision of multiple bumps may also be beneficial where intermittent unidirectional currents are provided through a pad (such as a pad providing a Pulse Width Modulation signal) and/or where bi-directional currents which are predominate in one direction are provided through a pad

(such as a pad providing a Pulse-Reverse Plating signal). In addition, provision of multiple bumps may be beneficial wherein sufficiently high AC currents are provided through a pad such that vacancies may accumulate at a solder bump interface during half cycles of the signal.

[0051] By providing a plurality of solder bumps connected to a same pad such as a ground pad, a Vcc pad, and/or an input/output pad, a device lifetime may be increased. More particularly, different resistances may be provided between the pad and each of the solder bumps connected to the pad so that, initially, current predominantly flows between the pad and a first solder bump connected through a path of least electrical resistance. Accordingly, vacancies (due to electromigration) may initially accumulate between the first solder bump and the respective under bump metallurgy layer, and vacancies may not substantially accumulate at a second solder bump connected through a path of higher resistance while the first solder bump is operational. The accumulation of vacancies at the first solder bump may eventually result in a void at the first solder bump and then failure of the first solder bump. Because significant current may not flow through the second solder bump until the first solder bump fails (due to the higher electrical resistance between the second solder bump and the pad), vacancies may not begin to significantly accumulate at the second solder bump until after failure of the first solder bump. An initiation of incubation of vacancies and/or voids in the second solder bump may thus be substantially delayed until after failure of the first solder bump. Stated in other words, initiation of a failure mechanism in the second solder bump may be substantially delayed until after failure of the first solder bump.

[0052] According to additional embodiments of the present invention, effects of electromigration can be reduced by providing a 'D' shaped via with a flat of the D facing the conductive line or trace (i.e. facing the incoming/outgoing current flow). This structure may reduce current crowding at a short path to a nearest point of a conventional circular via. In an alternative, the via can be concave and/or crescent shaped in the direction of the conductive line or trace (i.e. in the direction of the incoming/outgoing current flow.

[0053] As shown in the top view of Figure 1A, a conductive line (or trace) **905** (such as a redistribution routing line) may be coupled to a circular conductive pad

903. The conductive line **905**, for example, may provide electrical interconnection between the conductive pad **903** and an input/output pad of an integrated circuit device, and a solder bump may be electrically coupled to the conductive pad **903**. Moreover, the conductive line **905** and pad **903** may be covered by a subsequently formed insulating layer, and a via hole **918** may be formed in the insulating layer so that edge (or peripheral) portions **903a** of the pad **903** remain covered by the insulating layer and central (or interior) portions **903b** are exposed by the via hole **918**. Stated in other words, central (or interior) portions **903b** of the conductive pad **903** may be free of the insulating layer.

[0054] As shown in Figure 1A, a perimeter of the via hole **918** may have a "D" shape as illustrated by the segments **917** and **917'**. Accordingly, a linear segment **917'** of the perimeter of the "D" shaped via hole **918** may be adjacent and/or closest to the conductive line (or trace) **905**. In an alternative, the perimeter of the via hole **918** may have a crescent shape as illustrated by the segments **917** and **917"**. Accordingly, a concave and/or crescent shaped segment **917"** of the via hole **918** may be adjacent and/or closest to the conductive line **905**.

[0055] According to some embodiments of the present invention, a first segment **917** of the perimeter of the via hole **918** may substantially define an arc of a circle around central portions of the conductive pad **903**. In addition, a second segment **917'** or **917"** of the perimeter of the via hole **918** may substantially deviate from the circle around the central portion of the conductive pad **903**. Moreover, the second segment **917'** or **917"** of the perimeter of the via hole **918** may be adjacent a connection between the conductive line **905** and the conductive pad **903**. More particularly, the second segment of the perimeter of the via hole **918** may define a line as shown by the segment **917'**, and a length of the second segment **917'** may be at least as great as a width of the conductive line. In an alternative, the second segment **917"** of the perimeter of the via hole **918** may curve toward a center of the conductive pad **903**. According to some other embodiments of the present invention, at least a segment of the perimeter of the via hole may be non-circular.

[0056] The cross sectional view of Figure 1B illustrates the conductive line **905** and pad **903** in an electronic device including a substrate **901** and an insulating layer

907. The via hole **917** may expose a portion of the conductive pad **903B** having a "D" shape and/or a crescent shape. Stated in other words, a perimeter of the via hole **918** may have a "D" shape and/or a crescent shape.

[0057] The cross sectional view of Figure 1C illustrates the structure of Figure 1B with the under bump metallurgy (UBM) layer **911** and solder bump **920** formed thereon. As shown in Figure 1C, portions of the UBM layer **911** and the solder bump **920** may extend over portions of the insulating layer **907** outside the via hole. Accordingly, portions of the UBM layer **911** and the solder bump **920** extending on the insulating layer **907** may define a circle even though the via hole is not circular. Accordingly, a solder bump **920** having a circular footprint may be provided even though a perimeter of the via hole through the insulating layer **907** has a "D" shape and/or a crescent shape.

[0058] Elements of structures illustrated in Figures 1A-C may be formed as discussed, for example, in U.S. Patent Application No. 10/601,938 filed June 23, 2003, the disclosure of which is hereby incorporated herein in its entirety by reference. For example, the conductive line **905** and pad **903** may include a patterned layer(s) of a conductive material(s) such as copper, aluminum, nickel, titanium, and/or combinations and/or alloys thereof. The UBM layer **911** may include one or more of an adhesion layer (such as a layer(s) of titanium, tungsten, chrome, and/or combinations and/or alloys thereof); a plating conduction layer (such as a layer of copper having a thickness in the range of approximately 0.1 to approximately 0.5 micrometers); a conductive shunt layer (such as a layer of copper having a thickness in the range of approximately 1.0 to approximately 5.0 micrometers); and/or a barrier layer (such as a layer(s) of nickel, platinum, palladium, and/or combinations and/or alloys thereof). The solder bump **920** may include lead-tin solder, but other solders may be used.

[0059] Figures 2A-B illustrate current concentrations from a conductive line **905** (for example, a redistribution line) to a conductive pad **903** exposed through a crescent shaped via hole **918** with a concave segment **917"** of the crescent toward the current carrying conductive line **905**. As shown in Figure 2A, a concentration of current entering/leaving the solder bump through the conductive pad **903** may be reduced. As shown in Figure 2A, a greatest concentration of current may be provided through the

conductive line **905**, and least concentrations of current may be provided at portions of the conductive pad **903** opposite the conductive line **905** and at a central portion **933** of the via hole. Greyscale shading between the conductive line **905** and the concave segment **917"** of the crescent illustrates a spreading (reduced concentration) of current entering/leaving the solder bump relative to a pad with a via hole having a circular perimeter.

[0060] Particular embodiments of the present invention including "D" shaped and crescent shaped vias are discussed above with respect to Figures 1A-C and 2A-B by way of example. Vias having other shapes and/or deviating from the particular shapes of Figures 1A-C and 2A-B may be provided according to other embodiments of the present invention. For example, sharp transitions of the perimeter of the via may be rounded either intentionally and/or as a result of processing tolerances.

[0061] According to additional embodiments of the present invention, increased solder bump life may be provided by reserving backup bumps that pass little current until a respective primary bump fails. Because nucleation of voids proceeds at a rate slower than void growth, relatively little nucleation may occur in a backup bump until the primary bump fails, and void nucleation in the backup bump may not substantially begin until after failure of the first bump when the backup bump begins carrying significant current. More particularly, separate redistribution lines may be provided from an integrated circuit contact pad to primary and backup solder bumps, and the redistribution line to the backup solder bump may provide a higher resistance than the redistribution line to the primary solder bump so that during normal operation, the backup solder bump carries significantly less current than the primary solder bump. For example, the redistribution line to the backup solder bump may be narrower, thinner, and/or longer than the redistribution line to the primary solder bump. Accordingly, the redistribution line to the backup solder bump may provide a resistance sufficiently greater than that of the redistribution line to the primary solder bump so that the primary solder bump carries significantly more current during normal operations. The resistance of the redistribution line to the backup solder bump, however, is sufficiently low so that performance of the integrated circuit device is not significantly diminished on failure of the primary solder bump. A failure mechanism resulting from void nucleation and

growth in the backup solder bump may thus not substantially begin until after failure of the primary solder bump.

[0062] While not shown in Figures 1A-C and 2A-B, the conductive line **905** may be coupled to an input/output pad on the substrate **901**. The conductive line **905** may be coupled to an input/output pad as shown, for example, in Figures 5A-B, 6A-B, 7A-B, 8A-B, 9A-B, and/or 10A-B. Moreover, the conductive line **905** may be one of a plurality of conductive lines coupled to a same input/output pad so that there is a redundancy of electrical connection between a single input/output pad and a next level of packaging.

[0063] As shown in the top view of Figure 7A and the cross sectional view of Figure 7B, a relatively short conductive line (or trace) **7001** may be provided between input/output pad **7003** and primary solder bump **7005**, and a relatively long conductive line (or trace) **7007** may be provided between input/output pad **7003** and backup solder bump **7009**. The greater length of conductive line **7007** relative to conductive line **7001** may provide a lesser resistance between input/output pad **7003** and primary solder bump **7005** than between input/output pad **7003** and secondary solder bump **7009**. Accordingly, current into and out of the input/output pad **7003** may flow primarily through conductive line **7001** and primary bump **7005** providing a path of least resistance. In the event of failure of a joint with the primary bump **7005**, current may then pass through conductive line **7007** and secondary bump **7009**.

[0064] As further shown in Figure 7B, the conductive lines **7001** and **7007** may be provided between first and second insulating layers **7111** and **7115**, and input/output pad **7003** may be provided between semiconductor substrate **7117** and first insulating layer **7111**. Moreover, via holes in the second insulating layer **7115** may expose conductive pads **7001'** and **7007'** respectively connected to conductive lines **7001** and **7007**, and under bump metallurgy layers **7121** and **7123** may be provided between solder bumps **7005** and **7009** and the respective conductive pads **7001'** and **7007'** of conductive lines **7001** and **7007**.

[0065] While not shown in Figures 7A-B, one or both of the via holes through the insulating layer **7115** exposing conductive pads **7001'** and/or **7007'** may have a non-circular perimeter as discussed above with respect to Figures 1A-C. More particularly,

one or both of the via holes through the insulating layer **7115** exposing conductive pads **7001'** and/or **7007'** may have a "D" shaped and/or a crescent shaped perimeter as discussed above with respect to Figures 1A-C.

[0066] As shown in the top view of Figure 8A and the cross sectional view of Figure 8B, a relatively wide conductive line (or trace) **8001** may be provided between input/output pad **8003** and primary solder bump **8005**, and a relatively narrow conductive line (or trace) **8007** may be provided between input/output pad **8003** and backup solder bump **8009**. The greater width of conductive line **8007** relative to conductive line **8001** may provide a lesser resistance between input/output pad **8003** and primary solder bump **8005** than between input/output pad **8003** and secondary solder bump **8009**. Accordingly, current into and out of the input/output pad **8003** may flow primarily through conductive line **8001** and primary bump **8005** providing a path of least resistance. In the event of failure of a joint with the primary bump **8005**, current may then pass through conductive line **8007** and secondary bump **8009**.

[0067] As further shown in Figure 8B, the conductive lines **8001** and **8007** may be provided between first and second insulating layers **8111** and **8115**, and input/output pad **8003** may be provided between semiconductor substrate **8117** and first insulating layer **8111**. Moreover, via holes in the second insulating layer **8115** may expose conductive pads **8001'** and **8007'** respectively connected to conductive lines **8001** and **8007**, and under bump metallurgy layers **8121** and **8123** may be provided between solder bumps **8005** and **8009** and the respective conductive pads **8001'** and **8007'** of conductive lines **8001** and **8007**.

[0068] While not shown in Figures 8A-B, one or both of the via holes through the insulating layer **8115** exposing conductive pads **8001'** and/or **8007'** may have a non-circular perimeter as discussed above with respect to Figures 1A-C. More particularly, one or both of the via holes through the insulating layer **8115** exposing conductive pads **8001'** and/or **8007'** may have a "D" shaped and/or a crescent shaped perimeter as discussed above with respect to Figures 1A-C.

[0069] As shown in the top view of Figure 9A and the cross sectional view of Figure 9B, a relatively thick conductive line (or trace) **9001** may be provided between input/output pad **9003** and primary solder bump **9005**, and a relatively thin conductive

line (or trace) **9007** may be provided between input/output pad **9003** and backup solder bump **9009**. The greater thickness of conductive line **9007** relative to conductive line **9001** may provide a lesser resistance between input/output pad **9003** and primary solder bump **9005** than between input/output pad **9003** and secondary solder bump **9009**. Accordingly, current into and out of the input/output pad **9003** may flow primarily through conductive line **9001** and primary bump **9005** providing a path of least resistance. In the event of failure of a joint with the primary bump **9005**, current may then pass through conductive line **9007** and secondary bump **9009**. The primary and backup conductive lines may include a common conductive layer(s) **9031** which may be formed using a same deposition(s), and the primary conductive line may include an additional conductive layer(s) **9033** not included in the backup conductive line. In an alternative, layers of the primary and backup conductive lines may be separately formed to have different thicknesses. In yet another alternative, the primary and backup conductive lines may include different conductive materials providing different resistances.

[0070] As further shown in Figure 9B, the conductive lines **9001** and **9007** may be provided between first and second insulating layers **9111** and **9115**, and input/output pad **9003** may be provided between semiconductor substrate **9117** and first insulating layer **9111**. Moreover, via holes in the second insulating layer **9115** may expose conductive pads **9001'** and **9007'** respectively connected to conductive lines **9001** and **9007**, and under bump metallurgy layers **9121** and **9123** may be provided between solder bumps **9005** and **9009** and the respective conductive pads **9001'** and **9007'** of conductive lines **9001** and **9007**. Moreover, elements of embodiments illustrated in Figures 7A-B, 8A-B, and 9A-B may be combined.

[0071] While not shown in Figures 9A-B, one or both of the via holes through the insulating layer **9115** exposing conductive pads **9001'** and/or **9007'** may have a non-circular perimeter as discussed above with respect to Figures 1A-C. More particularly, one or both of the via holes through the insulating layer **9115** exposing conductive pads **9001'** and/or **9007'** may have a "D" shaped and/or a crescent shaped perimeter as discussed above with respect to Figures 1A-C.

[0072] As shown in the top view of Figure 10A and the cross sectional view of Figure 10B, a plurality of solder bumps **10005a-c** may be provided along a same conductive line (or trace) including segments **10001a-c** connected to input/output pad **10003**. The lesser distance between the solder bump **10005a** and the input/output pad **10003** relative to the solder bumps **10005b-c** may provide a lesser resistance between input/output pad **10003** and primary solder bump **10005a** than between input/output pad **10003** and secondary solder bumps **10005b** or **10005c**. Accordingly, current into and out of the input/output pad **10003** may flow primarily through primary bump **10005a** providing a path of least resistance. In the event of failure of a joint with the primary bump **10005a**, current may then pass through conductive line segments **10001a-b** and secondary bump **10005b**. In the event of failure of a joint with the primary bump **10005a** and the first secondary bump **10005b**, current may then pass through conductive line segments **10001a-c** and second secondary bump **10005c**.

[0073] As further shown in Figure 10B, the conductive line segments **10001a-c** may be provided between first and second insulating layers **10111** and **10115**, and input/output pad **10003** may be provided between semiconductor substrate **10117** and first insulating layer **10111**. Moreover, via holes in the second insulating layer **10115** may expose conductive pads **10001a'**, **10001b'**, and **10001c'** respectively connected to the conductive line including segments **10001a-c**, and under bump metallurgy layers **10121a-c** may be provided between solder bumps **10005a-c** and the respective conductive pads **10001a'-c'**.

[0074] Moreover, the different segments **10001a-c** of the conductive line may have different properties to provided further increases in resistance between solder bumps more distantly located from the input/output pad **10003**. For example, a width of the segment **10001a** may be greater than a width of the segment **10001b**, and/or a width of the segment **10001b** may be greater than a width of the segment **10001c**. In addition or in an alternative, a thickness of the segment **10001a** may be greater than a thickness of the segment **10001b**, and/or a thickness of the segment **10001b** may be greater than a thickness of the segment **10001c**. Moreover, a length of the segment **10001a** may be less than a length of the segment **10001b**, and/or a length of the segment **10001b** may be less than a length of the segment **10001c**.

[0075] While not shown in Figures 10A-B, one or both of the via holes through the insulating layer **10115** exposing conductive pads **10001a'-c'** may have a non-circular perimeter as discussed above with respect to Figures 1A-C. More particularly, one or both of the via holes through the insulating layer **10115** exposing conductive pads **10001a'-c'** may have a "D" shaped and/or a crescent shaped perimeter as discussed above with respect to Figures 1A-C.

[0076] As used herein, the term under bump metallurgy layer refers to one or more conductive layers provided between a solder bump and a substrate. An under bump metallurgy layer may include an adhesion layer (such as a layer of titanium, tungsten, chrome, and/or combinations thereof), a conduction layer (such as a layer of copper), and/or a barrier layer (such as a layer of nickel, platinum, palladium, and/or combinations thereof). A solder bump may be a bump of one or more different solder materials. For example, a solder bump may include one or more of a single element, binary, ternary, and/or higher order solder; such as a lead-tin solder, a lead-bismuth solder, a lead-indium solder, a lead free solder, a tin-silver solder, a tin-silver-copper solder, an indium-tin solder, an indium-gallium solder, a gallium solder, an indium-bismuth solder, a tin-bismuth solder, an indium-cadmium solder, bismuth-cadmium solder, tin-cadmium, etc. Accordingly, an under bump metallurgy layer may provide a surface that is wettable to a solder bump wherein the solder wettable surface of the under bump metallurgy layer and the solder bump comprise different materials.

[0077] While the present invention has been particularly shown and described with reference to embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims and their equivalents.

That Which Is Claimed Is:

1. An integrated circuit device comprising:

a substrate;

a conductive pad on a surface of the substrate;

a conductive line on the surface of the substrate wherein the conductive line is connected to the conductive pad and wherein the conductive line is narrow relative to the conductive pad; and

an insulating layer on the substrate, on the conductive line, and on edge portions of the conductive pad wherein the insulating layer has a hole therein exposing a central portion of the conductive pad, and wherein a first segment of a perimeter of the hole substantially defines an arc of a circle around the central portion of the conductive pad and wherein a second segment of the perimeter of the hole substantially deviates from the circle around the central portion of the conductive pad, and wherein the second segment of the perimeter of the hole is adjacent a connection between the conductive line and the conductive pad.

2. An integrated circuit device according to Claim 1 further comprising:

a conductive bump on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the insulating layer is between the conductive bump and edge portions of the conductive pad.

3. An integrated circuit device according to Claim 2 wherein the conductive bump comprises a solder bump.

4. An integrated circuit device according to Claim 2 wherein the conductive bump has a substantially circular footprint on the insulating layer.

5. An integrated circuit device according to Claim 2 further comprising:

an underbump metallurgy layer on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the under bump

metallurgy layer is between the conductive bump and portions of the insulating layer surrounding the hole, and wherein the underbump metallurgy layer and the conductive bump comprise different materials.

6. An integrated circuit device according to Claim 1 further comprising:

an input/output pad on the substrate wherein the conductive line provides electrical connection between the conductive pad and the input/output pad.

7. An integrated circuit device according to Claim 6 further comprising:

a second conductive line connected to the input/output pad;

a second conductive pad connected to the second conductive line wherein the insulating layer has a second hole therein exposing a central portion of the second conductive pad;

a first conductive bump on the central portion of the first conductive pad and on portions of the insulating layer surrounding the first hole; and

a second conductive bump on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole.

8. An integrated circuit device according to Claim 1 wherein the second segment of the perimeter of the hole substantially defines a line.

9. An integrated circuit device according to Claim 8 wherein a length of the second segment is at least as great as a width of the conductive line.

10. An integrated circuit device according to Claim 1 wherein the second segment of the perimeter of the hole curves toward the center of the conductive pad.

11. An integrated circuit device comprising:

a substrate;

a conductive pad on a surface of the substrate;

a conductive line on the surface of the substrate wherein the conductive line is connected to the conductive pad and wherein the conductive line is narrow relative to the conductive pad;

an insulating layer on the substrate, on the conductive line, and on edge portions of the conductive pad wherein the insulating layer has a hole therein exposing a central portion of the conductive pad and wherein at least a segment of a perimeter of the hole is non-circular; and

a conductive bump on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the insulating layer is between the conductive bump and edge portions of the conductive pad and wherein the conductive bump has a substantially circular footprint on the insulating layer.

12. An integrated circuit device according to Claim 11 wherein the conductive bump comprises a solder bump.

13. An integrated circuit device according to Claim 11 further comprising:

an underbump metallurgy layer on the central portion of the conductive pad and on portions of the insulating layer surrounding the hole so that the under bump metallurgy layer is between the conductive bump and portions of the insulating layer surrounding the hole, and wherein the underbump metallurgy layer and the conductive bump comprise different materials.

14. An integrated circuit device according to Claim 11 wherein a first segment of a perimeter of the hole substantially defines an arc of a circle around the central portion of the conductive pad and wherein a second segment of the perimeter of the hole substantially deviates from the circle around the central portion of the conductive pad.

15. An integrated circuit device according to Claim 14 wherein the second segment of the perimeter of the hole is adjacent a connection between the conductive line and the conductive pad.

16. An integrated circuit device according to Claim 14 wherein the second segment of the perimeter of the hole substantially defines a line.

17. An integrated circuit device according to Claim 16 wherein a length of the second segment is at least as great as a width of the conductive line.

18. An integrated circuit device according to Claim 14 wherein the second segment of the perimeter of the hole curves toward the center of the conductive pad.

19. An integrated circuit device according to Claim 11 further comprising:

an input/output pad on the substrate wherein the conductive line provides electrical connection between the conductive pad and the input/output pad.

20. An integrated circuit device according to Claim 6 further comprising:

a second conductive line connected to the input/output pad;

a second conductive pad connected to the second conductive line wherein the insulating layer has a second hole therein exposing a central portion of the second conductive pad;

a first conductive bump on the central portion of the first conductive pad and on portions of the insulating layer surrounding the first hole; and

a second conductive bump on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole.

21. An integrated circuit device comprising

a substrate;

an input/output pad on the substrate;

first and second conductive lines on the substrate wherein both of the first and second lines are connected to the input/output pad;

first and second conductive pads on the substrate wherein the first conductive pad is connected to the first conductive line and wherein the second conductive pad is connected to the second conductive line;

an insulating layer on the first and second conductive lines and on edge portions of the first and second conductive pads wherein the insulating layer has first and second holes therein exposing central portions of the respective first and second conductive pads;

a first conductive bump on the central portion of the first conductive bump and on portions of the insulating layer surrounding the first hole; and

a second conductive bump on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole.

22. An integrated circuit device according to Claim 21 wherein the first and second conductive bumps comprise respective first and second solder bumps.

23. An integrated circuit device according to Claim 21 wherein each of the first and second conductive bumps has a substantially circular footprint on the insulating layer.

24. An integrated circuit device according to Claim 21 further comprising:

a first underbump metallurgy layer on the central portion of the first conductive pad and on portions of the insulating layer surrounding the first hole so that the first under bump metallurgy layer is between the first conductive bump and portions of the insulating layer surrounding the first hole wherein the first underbump metallurgy layer and the first conductive bump comprise different materials; and

a second underbump metallurgy layer on the central portion of the second conductive pad and on portions of the insulating layer surrounding the second hole so that the second under bump metallurgy layer is between the second conductive bump and portions of the insulating layer surrounding the second hole wherein the second underbump metallurgy layer and the second conductive bump comprise different materials.

25. An integrated circuit device according to Claim 21 wherein the first conductive line provides a first electrical resistance between the input/output pad and the first conductive pad, wherein the second conductive line provides a second electrical

resistance between the input/output pad and the second conductive pad, and wherein the first and second electrical resistances are different.

26. An integrated circuit device according to Claim 25 wherein the first conductive line has a first length between the input/output pad and the first conductive pad, wherein the second conductive line has a second length between the input/output pad and the second conductive pad, and wherein the first and second lengths are different.

27. An integrated circuit device according to Claim 25 wherein the first conductive line has a first width, wherein the second conductive line has a second width, and wherein the first and second widths are different.

28. An integrated circuit device according to Claim 25 wherein the first conductive line has a first thickness, wherein the second conductive line has a second thickness, and wherein the first and second thicknesses are different.

29. An integrated circuit device according to Claim 25 wherein the first conductive line comprises a first material, wherein the second conductive line comprises a second material, and wherein the first and second materials are different.

30. An integrated circuit device according to Claim 21 wherein the input/output pad comprises a ground pad providing a ground connection for the integrated circuit device.

31. An integrated circuit device according to Claim 21 wherein the input/output pad comprises a power pad providing a power connection for the integrated circuit device.

32. An integrated circuit device according to Claim 21 wherein the first conductive line is narrow relative to the first conductive pad, and wherein a first segment of a perimeter of the first hole substantially defines an arc of a circle around the central

portion of the first conductive pad and wherein a second segment of the perimeter of the first hole substantially deviates from the circle around the central portion of the conductive pad, and wherein the second segment of the perimeter of the first hole is adjacent a connection between the conductive line and the conductive pad.

33. An integrated circuit device according to Claim 21 wherein at least a segment of a perimeter of the first hole is non-circular.

34. An integrated circuit device according to Claim 21 wherein the first and second conductive lines are configured such that the first conductive bump fails due to electromigration before the second conductive bump fails.

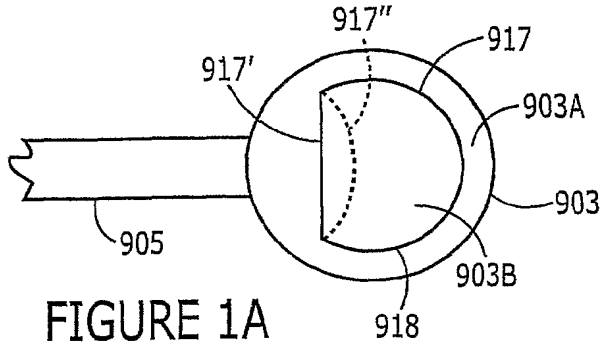

FIGURE 1A

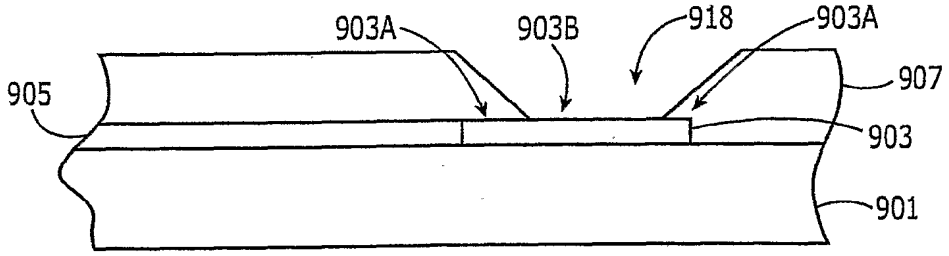

FIGURE 1B

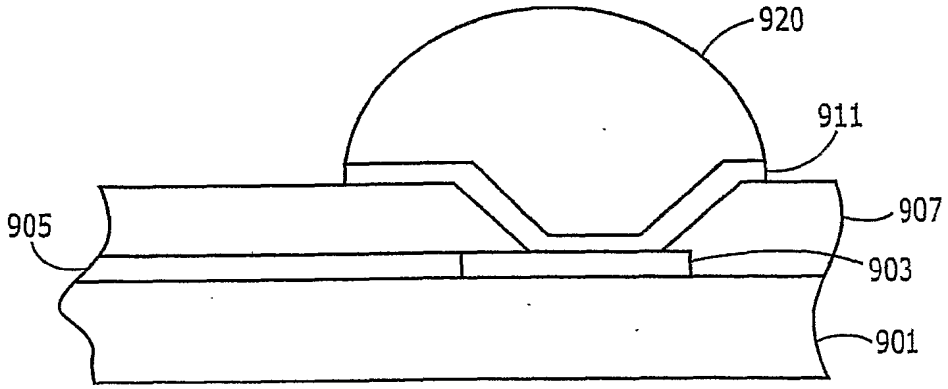

FIGURE 1C

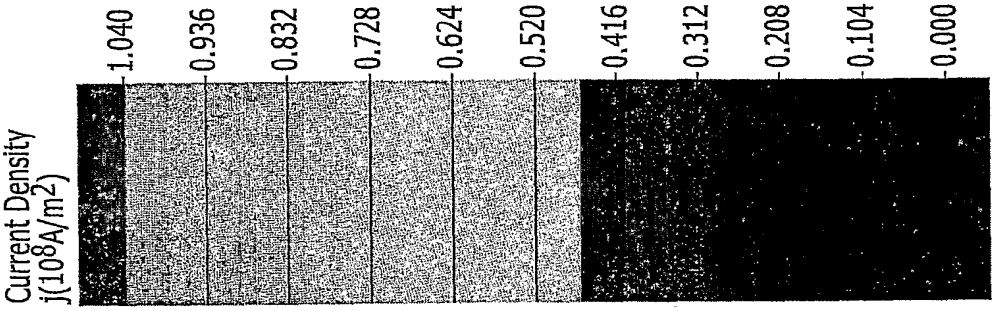

FIGURE 2B

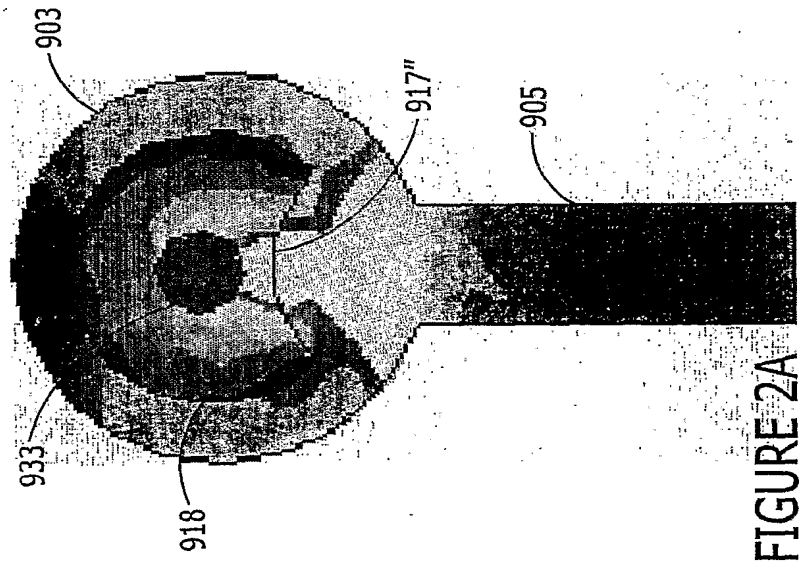

FIGURE 2A

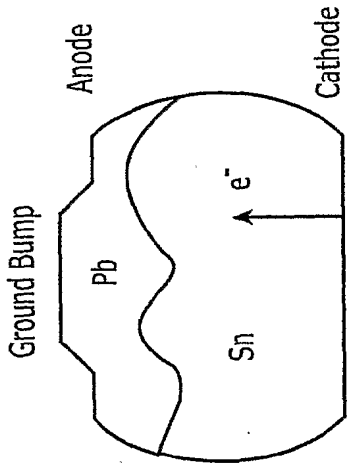

FIGURE 4A

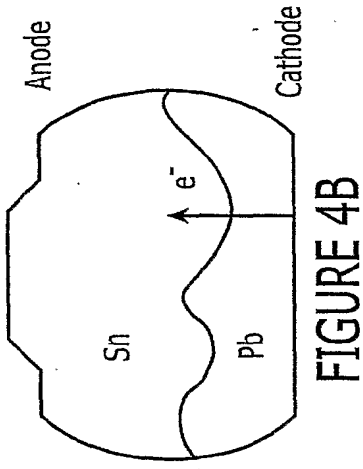

FIGURE 4B

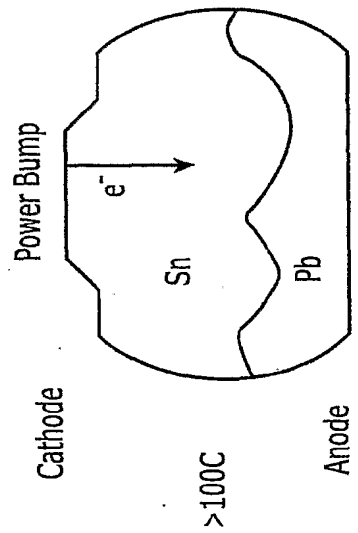

FIGURE 3A

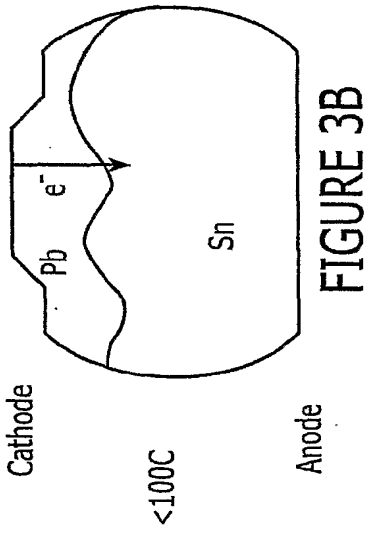

FIGURE 3B

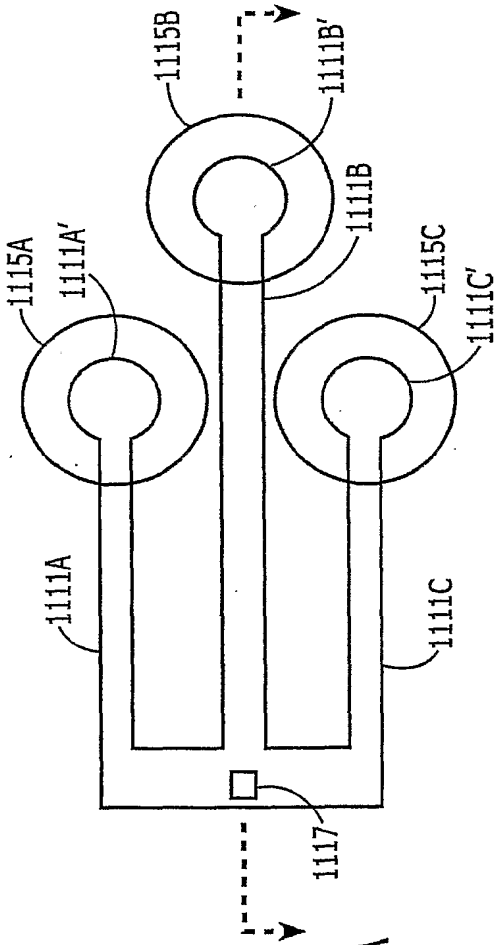

FIGURE 5A

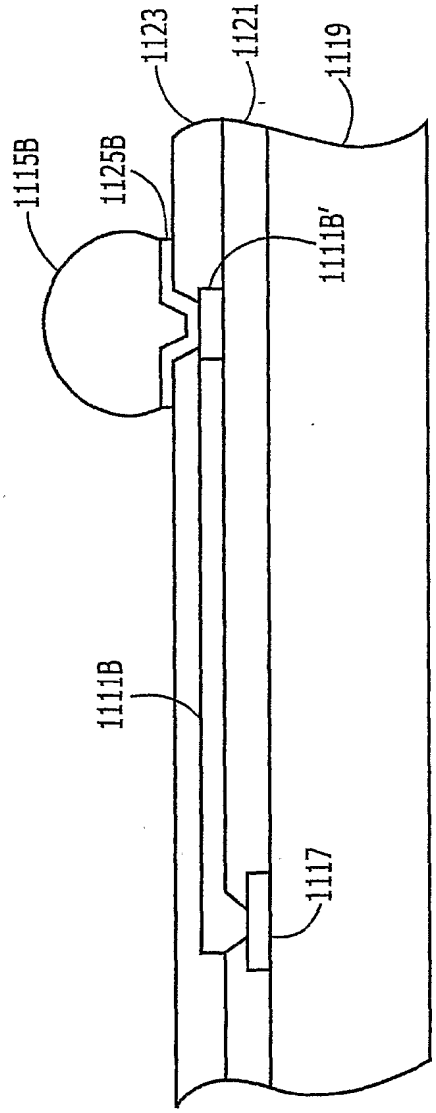

FIGURE 5B

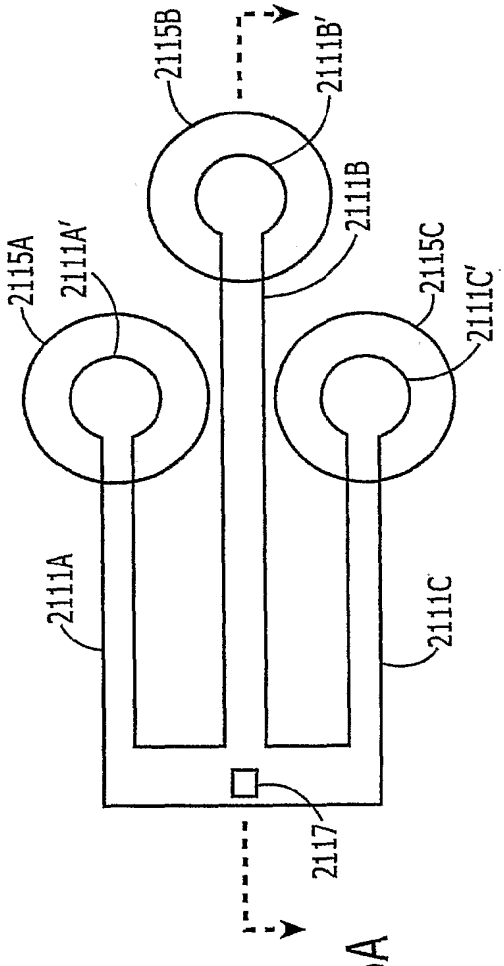

FIGURE 6A

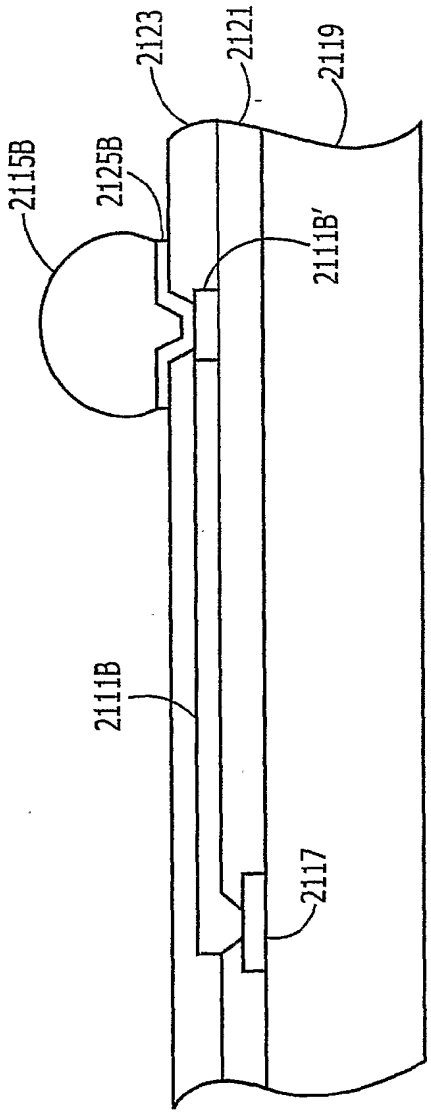

FIGURE 6B

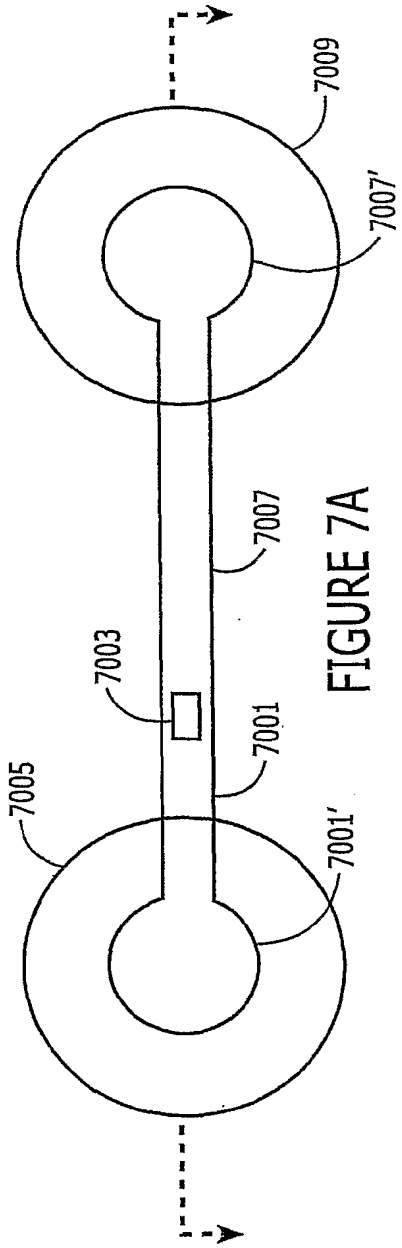

FIGURE 7A

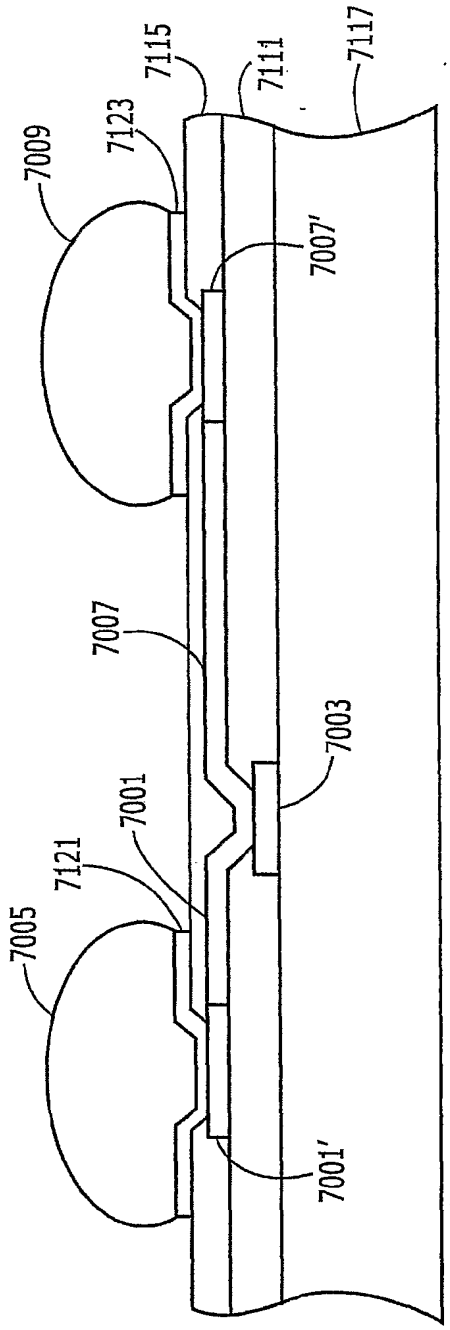

FIGURE 7B

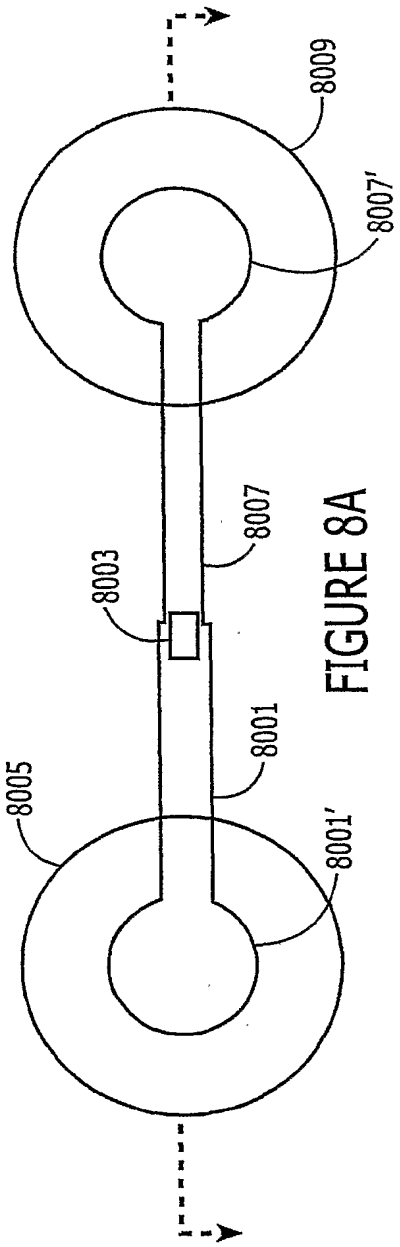

FIGURE 8A

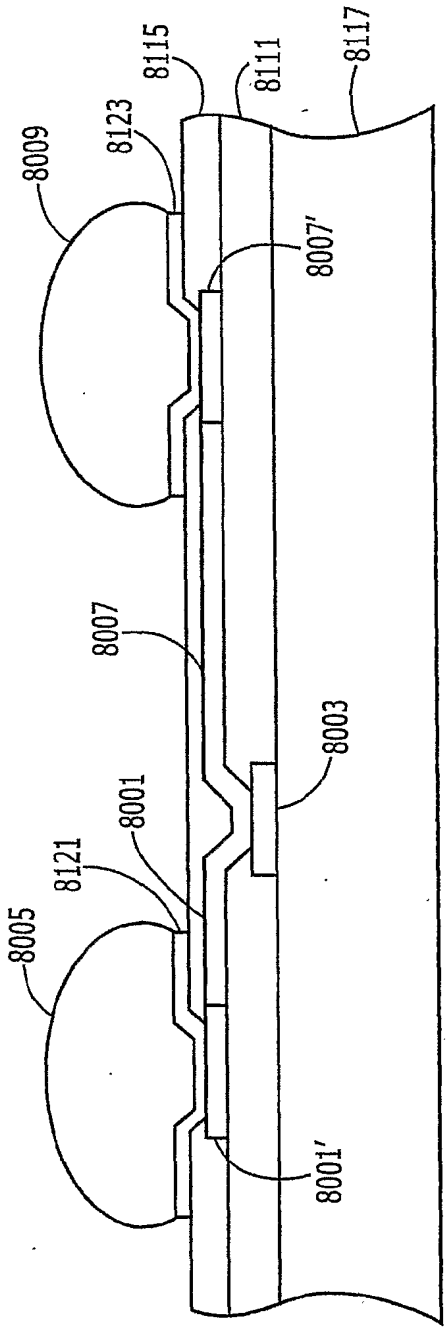

FIGURE 8B

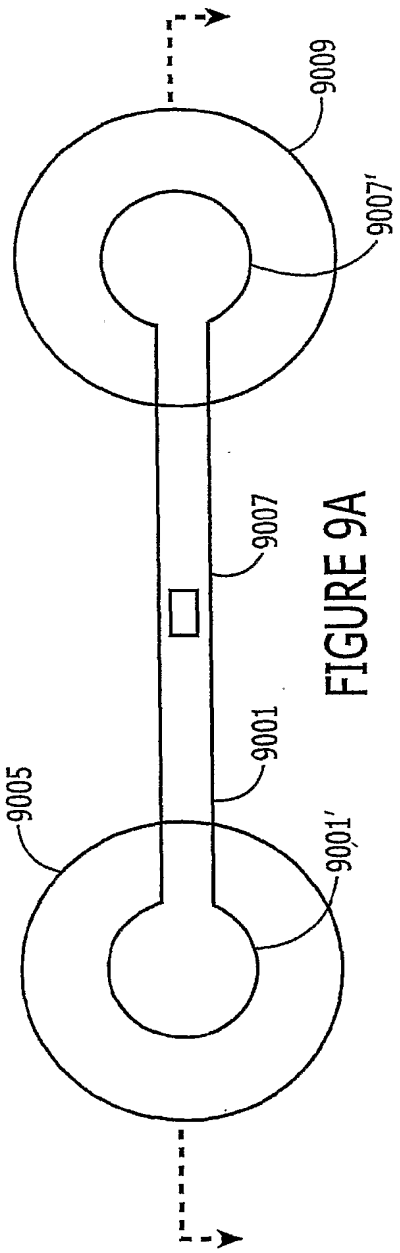

FIGURE 9A

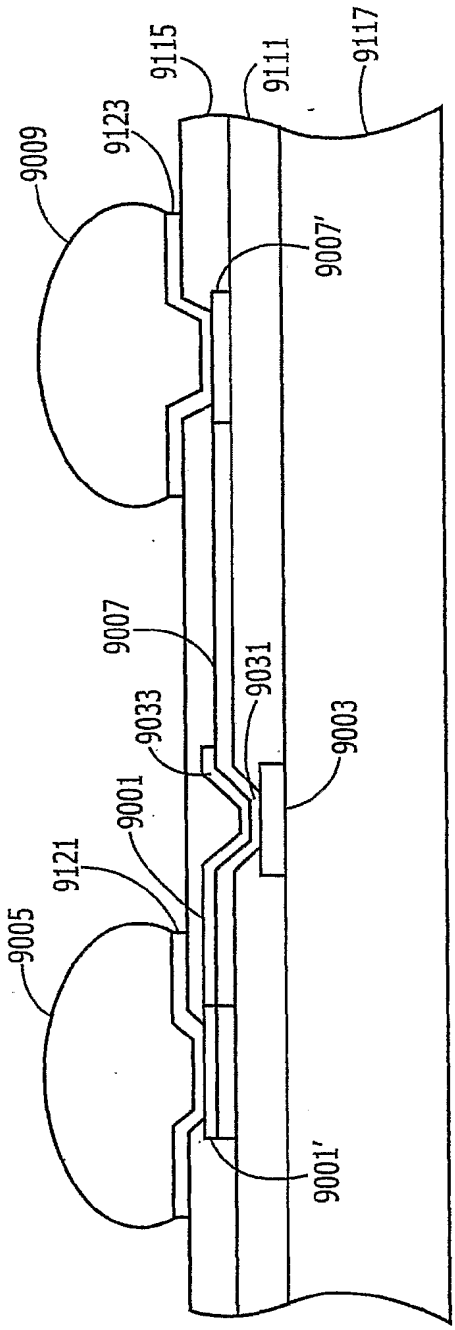

FIGURE 9B

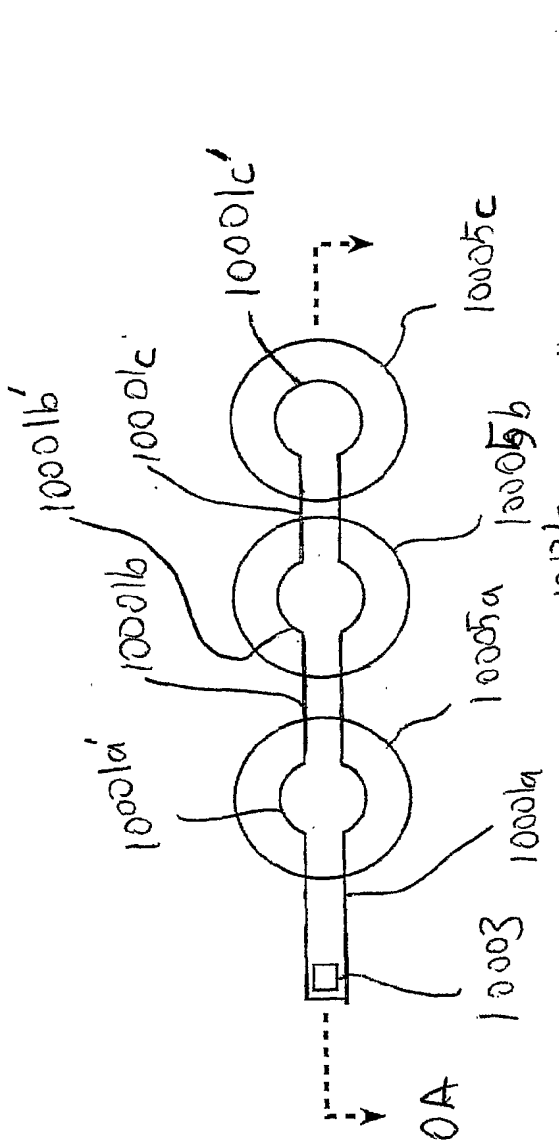

FIGURE 10A

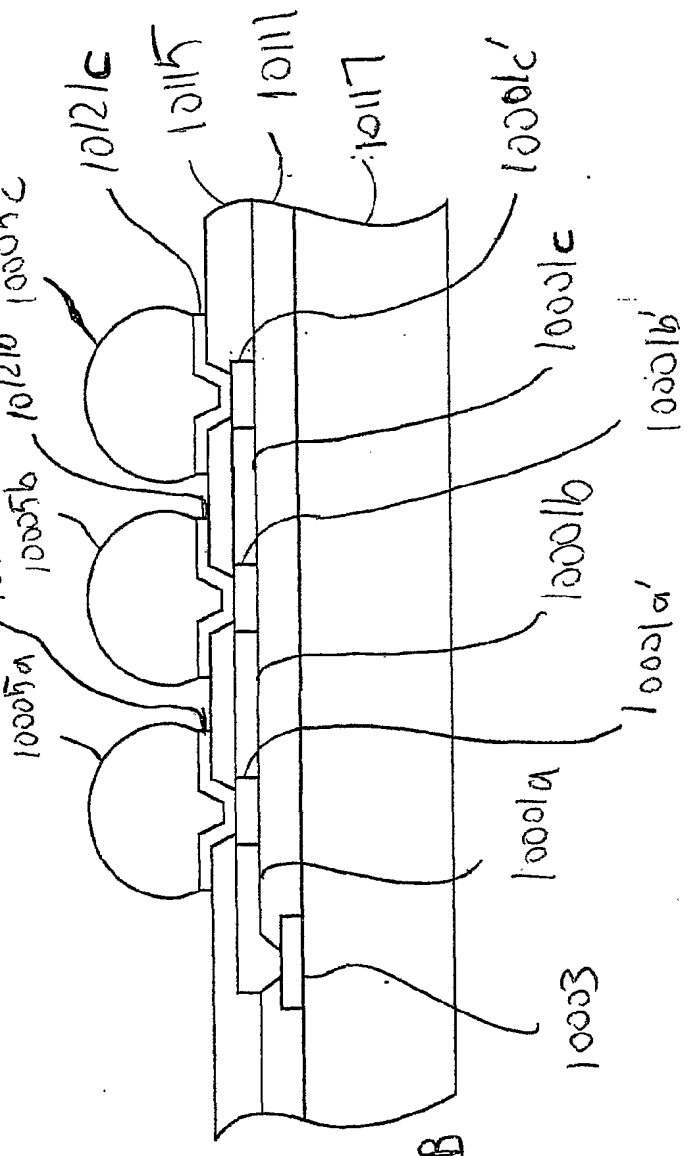

FIGURE 10B